Assignment for Lab 2 Weekly Lab Report Demo CMOS Transistor Level Current Source Design, Simulation and Experimental Test as well as Analysis

Diagram, schematic

Description automatically generated

Case 1 CMOS Mirror Normal Sizing

A picture containing chart

Description automatically generated

Table

Description automatically generated

Diagram, schematic

Description automatically generated

Table

Description automatically generated

Case 3 NMOS Bias Double Sizing

Timeline

Description automatically generated with low confidence

Table

Description automatically generated

Graph of NMOS BIAS Double Sizing

Diagram, schematic

Description automatically generated

Case 5 AC Current Mirror with Bias NMOS @ 2(W/L) @ 200 kHz

Chart

Description automatically generated with medium confidence

Table

Description automatically generated

Graphical representation of AC current Applied to Double Sized Biased NMOS Circuit